CLAIMS

What is claimed is:

1. An integrated circuit manufacturing process using data related to manufacturing procedures used previously that a plurality of integrated circuits of semiconductor devices have undergone for selecting manufacturing procedures a plurality of integrated circuits of a semiconductor devices are to undergo, each semiconductor device having integrated circuits and having a substantially unique identification code, the manufacturing process comprising:

storing data in association with the identification code of each semiconductor device identifying manufacturing procedures the semiconductor device has undergone;

automatically reading the identification code of each semiconductor device; and

accessing the data stored in association with the identification code of each semiconductor device.

2. The process of claim 1, further comprising:

selecting manufacturing procedures each semiconductor device undergoes in accordance with the accessed data.

3. The process of claim 1, wherein the step of storing data comprises storing data that identifies repairs performed semiconductor device.

4. The process of claim 3, wherein the semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein storing data comprises storing data that identifies spare rows and columns used in repairing the DRAM semiconductor device.

5. The process of claim 3, wherein the semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein storing data comprises storing data that identifies spare rows and columns available to effect repairs in the DRAM semiconductor device.

6. The process of claim 1, wherein the step of storing data comprises storing data at probe.

7. The process of claim 1, wherein the step of automatically reading the identification code of each semiconductor device comprises electrically retrieving a unique fuse ID programmed into each semiconductor device.

8. The process of claim 1, wherein the step of automatically reading the identification code of each semiconductor device comprises optically reading a unique ID code provided on each semiconductor device.

9. The process of claim 8, wherein the step of optically reading a unique identification code provided on each semiconductor device comprises optically reading a unique laser fuse ID programmed into each semiconductor device.

10. The process of claim 1, wherein the step of automatically reading the identification code of each semiconductor device comprises automatically reading the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the semiconductor device manufacturing process.

11. The process of claim 1, wherein the step of accessing the data stored in association with the identification code of each semiconductor device comprises accessing the data stored in association with the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the semiconductor device manufacturing process.

12. The process of claim 2, wherein selecting manufacturing procedures the semiconductor device undergoes in accordance with the accessed data comprises selecting repairs the semiconductor device undergoes in accordance with the accessed data.

13. The process of claim 12, wherein the semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein selecting repairs the semiconductor device undergoes comprises selecting spare rows and columns used to repair the DRAM semiconductor device.

14. The process of claim 2, wherein the step of selecting manufacturing procedures the semiconductor device undergoes in accordance with the accessed data comprises selecting whether the semiconductor device undergoes repair procedures.

15. The process of claim 14, wherein the semiconductor device comprise Dynamic Random Access Memory (DRAM) semiconductor device, wherein selecting whether the semiconductor device undergoes repair procedures comprises selecting whether the DRAM semiconductor device will be repaired in accordance with whether the accessed data indicates enough spare rows and columns are available in the semiconductor device to effect repairs.

16. The process of claim 2, wherein the step of selecting manufacturing procedures the semiconductor device will undergo in accordance with the accessed data comprises determining whether the semiconductor device will be assembled into Multi-Chip Modules (MCM's) in accordance with whether the accessed data indicates the semiconductor device is repairable.

17. The process of claim 1, further comprising assembling the semiconductor device into a packaged semiconductor device after the step of storing data and before the step of automatically reading the identification code of each semiconductor device.

18. A method of manufacturing integrated circuit semiconductor devices from semiconductor wafers, the method comprising:
providing a plurality of semiconductor wafers;
fabricating a plurality of semiconductor devices on each of the wafers;

causing each semiconductor device on each of the wafers to store a substantially unique identification code;

storing data in association with the identification code of each semiconductor device that identifies manufacturing procedures the semiconductor device has undergone;

separating each semiconductor device on each of the wafers from its wafer to form one semiconductor device of a plurality of semiconductor dice;

assembling each semiconductor device into a semiconductor device assembly;

automatically reading the identification code associated with each semiconductor device; and

accessing the data stored in association with the identification code associated with each semiconductor device.

19. The method of claim 18, further comprising:

selecting manufacturing procedures the semiconductor device undergoes in accordance with the accessed data.

20. The method of claim 18, wherein the step of fabricating a plurality of semiconductor devices on each of the wafers comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor device, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, and processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices .

21. The method of claim 18, wherein the step of causing each semiconductor device on each of the wafers to store a substantially unique identification code comprises programming each semiconductor device on each of the wafers to permanently store a unique fuse ID.

22. The method of claim 18, wherein the step of programming each semiconductor device on each of the wafers to permanently store a unique fuse identification code comprises programming at least one of fuses and anti-fuses in each semiconductor device on each of the wafers to permanently store a unique fuse identification.

23. The method of claim 18, wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

picking each semiconductor device from its wafer;

placing each semiconductor device onto an epoxy coated bonding site of one lead frame of a plurality of lead frames;

curing the epoxy on the bonding site of each lead frame of the lead frames;

wire bonding each semiconductor device to its associated lead frame;

encapsulating each semiconductor device and its associated lead frame to form one of a plurality of semiconductor device assembly packages, each package having projecting leads;

curing each of the semiconductor device assembly packages;

de-flashing the projecting leads of each semiconductor device assembly package;

electroplating the projecting leads of each semiconductor device assembly package; and

singulating each semiconductor device assembly package into one semiconductor device assembly package of a plurality of discrete semiconductor device assembly packages.

24. The method of claim 18, wherein the step of assembling each semiconductor device into a semiconductor device assembly comprises assembling each semiconductor device into a semiconductor device assembly selected from a group comprising a wire bond/lead frame semiconductor device, a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

25. A method of manufacturing Multi-Chip Modules (MCM's) from semiconductor wafers, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each of the wafers;

causing each semiconductor device of the semiconductor devices on each of the wafers to store a substantially unique identification code;

storing data in association with the identification code of each semiconductor device of the semiconductor devices that identifies manufacturing procedures each semiconductor device of semiconductor devices has undergone;

separating each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers from its wafer to form one semiconductor device of a plurality of semiconductor devices;

assembling one or more of the semiconductor devices into each of a plurality of MCM's;

automatically reading the identification code of each semiconductor device of the semiconductor devices in each MCM of the plurality of MCM's; and

accessing the data stored in association with the identification code of each semiconductor device of the semiconductor devices in each MCM of the plurality of MCM's.

26. The method of claim 25, further comprising:

selecting manufacturing procedures the semiconductor devices will undergo in accordance with the accessed data.

27. The method of claim 25, wherein the MCM's are selected from a group comprising Single In-Line Memory Modules (SIMM's) and Dual In-line Memory Modules (DIMM's), Rambus In-Line Memory Modules (RIMM), Small Outline Rambus In-Line Memory Modules (SO-RIMM), Personal Computer Memory Format (PCMCIA), and Board-Over-Chip type substrate.

28. A method of manufacturing semiconductor devices from semiconductor wafers, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each of the wafers;

electronically probing each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers to identify good, bad and repairable semiconductor devices on each wafer of the plurality of semiconductor wafers;

repairing the repairable semiconductor devices;

programming each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers to store a unique fuse identification;

storing data in association with the fuse identification of each of the semiconductor devices identifying repairs performed on each semiconductor device of the semiconductor devices;

mounting each wafer of the plurality of semiconductor wafers on an adhesive film;

sawing each semiconductor device of the semiconductor devices on each wafer of the plurality of wafers from its wafer to form one of a plurality of discrete semiconductor devices;

automatically picking each semiconductor device of the semiconductor devices from its wafer;

placing each semiconductor device of the semiconductor devices onto an epoxy coated bonding site of one lead frame of a plurality of lead frames;

curing the epoxy on the bonding site of each lead frame of the lead frames;

wire bonding each semiconductor device of the semiconductor devices to its associated lead frame;

encapsulating each semiconductor device of the semiconductor devices and its associated lead frame to form one of a plurality of semiconductor device assembly packages each semiconductor device assembly package having projecting leads;

curing each semiconductor device assembly package;

de-flashing the projecting leads of each semiconductor device package;

electroplating the projecting leads of each semiconductor device package;

singulating each semiconductor device package;

testing each semiconductor device assembly package for opens and shorts;

burn-in testing each semiconductor device assembly package;

back-end testing each semiconductor device assembly package;

automatically reading the identification code of each semiconductor device assembly package;

accessing the data stored in association with the identification code of each semiconductor device assembly package;

for any semiconductor device assembly package failing any one of the opens/shorts, burn-in, and back-end tests, evaluating the accessed data to determine whether the failing semiconductor device assembly package may be repaired;

repairing any of the semiconductor device assembly package determined in accordance with the accessed data to be repairable and returning the repaired semiconductor device assembly package to the semiconductor manufacturing process; and

discarding any of the semiconductor device assembly package determined in accordance with the accessed data to be unrepairable.

29. The method of claim 28, wherein the step of mounting the wafers comprises mounting each wafer of the plurality of semiconductor wafers on an ultraviolet (U.V.) adhesive film, wherein the method further comprises exposing the U.V. adhesive film to U.V. light to loosen the wafers from the film prior to picking and placing the semiconductor device.

30. The method of claim 28, further comprising receiving a plurality of unrepairable semiconductor devices diverted from another semiconductor device manufacturing process.

31. A method of manufacturing Multi-Chip Modules (MCM's) from semiconductor wafers using Chip-On-Board (COB) techniques, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each wafer of the plurality of semiconductor wafers;

electronically probing each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers to identify good, bad and repairable semiconductor devices on each wafer of the plurality of semiconductor wafers;

repairing the repairable semiconductor devices;

programming each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers to store a unique fuse identification;

storing an electronic wafer map for each wafer that identifies the locations of good and bad semiconductor devices on the wafer and associates each unique fuse identification on the wafer with its fuse identification code;

storing data in association with the fuse identification code of each semiconductor device of the semiconductor devices identifying repairs performed on each semiconductor device of the semiconductor devices;

mounting each wafer of the plurality of semiconductor wafers on an adhesive film;

sawing each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers from its wafer to form one discrete semiconductor device;

accessing the stored wafer map for each wafer;

accessing the stored data for each semiconductor device on each wafer of the plurality of semiconductor wafers;

automatically picking each semiconductor device of the good semiconductor devices from its wafer;

discarding non-picked semiconductor devices identified as bad by the accessed wafer maps;

diverting picked semiconductor devices identified as good but unrepairable by the accessed wafer maps and data to a non-MCM semiconductor manufacturing process;

placing picked semiconductor devices identified as good and repairable by the accessed wafer maps and data onto epoxy coated bonding sites of a plurality of printed circuit boards using COB techniques to form a plurality of MCM's;

curing the epoxy on the bonding sites of each MCM of the plurality of MCM's;

wire bonding each of the semiconductor devices to its associated MCM;

testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's for opens and shorts;

encapsulating each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

retesting each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's for opens and shorts;

burn-in testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

back-end testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

automatically reading the fuse identification code of each semiconductor device in each MCM of the plurality of MCM's;

accessing the data stored in association with the fuse identification code of each semiconductor device of the semiconductor devices;

for any semiconductor device of the semiconductor devices failing any one of the opens/shorts, burn-in, and back-end tests, evaluating the accessed data to determine whether the failing semiconductor device may be repaired;

repairing any semiconductor device of the semiconductor devices determined in accordance with the accessed data to be repairable and returning the repaired MCM to the manufacturing process; and

replacing any semiconductor device of the semiconductor devices determined in accordance with the accessed data to be unrepairable with Known Good Die (KGD) dice and returning the repaired MCM to the manufacturing process.

32. The method of claim 31, further comprising plasma cleaning each MCM of the plurality of MCM's after curing the epoxy on the bonding sites of the MCM.

33. The method of claim 31, wherein the step of mounting the wafers comprises mounting each wafer of the plurality of semiconductor wafers on an Ultraviolet (U.V.) adhesive film, wherein the method further comprises exposing the U.V. adhesive film to U.V. light to loosen the wafer from the film prior to picking and placing the semiconductor device.

34. The method of claim 31, further comprising singulating the printed circuit boards associated with each MCM of the plurality of MCM's.

35. A method of manufacturing Multi-Chip Modules (MCM's) from semiconductor wafers using flip-chip techniques, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each wafer of the semiconductor wafers;

electronically probing each semiconductor device of the semiconductor devices on each wafer of the plurality of wafers to identify good, bad and repairable semiconductor devices on each wafer of the plurality of wafers;

repairing the repairable semiconductor devices;

programming each semiconductor device of the semiconductor devices on each wafer of the plurality of wafers to store a unique fuse identification;

storing an electronic wafer map for each wafer that identifies the locations of good and bad semiconductor devices on the wafer and associates each semiconductor device on the wafer with its fuse identification;

storing data in association with the fuse identification of each semiconductor device of the semiconductor devices identifying repairs performed on each semiconductor device of the semiconductor devices;

mounting each wafer of the plurality of wafers on an adhesive film;

sawing each semiconductor device of the semiconductor devices on each wafer of the wafers from its wafer to form a semiconductor device;

accessing the stored wafer map for each wafer;

accessing the stored data for each semiconductor device of the semiconductor devices on each of the wafers;

automatically picking each semiconductor device of the good semiconductor devices from its wafer;

discarding non-picked semiconductor devices identified as bad by the accessed wafer maps;

diverting picked semiconductor devices identified as good but unrepairable by the accessed wafer maps and data to a non-MCM device manufacturing process;

flip-chip attaching picked semiconductor devices identified as good and repairable by the accessed wafer maps and data to bonding sites of each printed circuit board of a plurality of printed circuit boards to form a plurality of MCM's;

curing each MCM of the plurality of MCM's;

testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's for opens and shorts;

encapsulating each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

retesting each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's for opens and shorts;

burn-in testing each semiconductor device of the semiconductor devices on each MCM of the plurality MCM's;

back-end testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

automatically reading the fuse identification code of each semiconductor device of the semiconductor devices in each MCM of the plurality of MCM's;

accessing the data stored in association with the fuse identification code of each semiconductor device of the semiconductor devices;

for any semiconductor device of the semiconductor devices failing any one of the opens/shorts, burn-in, and back-end tests, evaluating the accessed data to determine whether the failing semiconductor devices may be repaired;

repairing any semiconductor device of the semiconductor devices determined in accordance with the accessed data to be repairable and returning the repaired MCM to the manufacturing process; and

replacing any semiconductor device of the semiconductor devices determined in accordance with the accessed data to be unrepairable with Known Good Die (KGD) die and returning the repaired MCM to the manufacturing process.

36. The method of claim 35, wherein the step of mounting the wafers comprises mounting each wafer of the plurality of wafers on an Ultraviolet (U.V.) adhesive film, wherein the method further comprises exposing the U.V. adhesive film to U.V. light to loosen the wafer from the film prior to picking and flip-chip attaching the semiconductor device.

37. The method of claim 35, further comprising singulating the printed circuit boards associated with each MCM of the plurality of MCM's.

38. A method in an integrated circuit semiconductor device in a Multi-Chip Module (MCM) manufacturing process for diverting good but unrepairable semiconductor devices from the process, the semiconductor devices being of the type to have a substantially unique identification code, the method comprising:

storing data in association with the identification code of each semiconductor device of the semiconductor devices identifying semiconductor devices that are good and repairable, that are good but unrepairable, and that are bad;

automatically reading the identification code of each semiconductor device of the semiconductor devices;

accessing the data stored in association with the identification code of each semiconductor device of the semiconductor devices;

diverting semiconductor devices identified as good but unrepairable by the accessed data to other semiconductor device manufacturing processes; and

discarding semiconductor devices identified as bad by the accessed data.

39. The method of claim 38, further comprising:

assembling at least one semiconductor device identified as good and repairable into at least one MCM.

40. A semiconductor device manufacturing process using data related to manufacturing procedures used previously that a plurality of integrated circuits of semiconductor devices have undergone for selecting manufacturing procedures a plurality of integrated circuits of a semiconductor devices are to undergo during manufacture, each semiconductor device having integrated circuits and having a substantially unique identification code, the manufacturing process comprising:

storing data in association with the identification code of each semiconductor device identifying manufacturing procedures the semiconductor device has undergone;

automatically reading the identification code of each semiconductor device; and

accessing the data stored in association with the identification code of each semiconductor device.

41. The process of claim 40, further comprising:

selecting manufacturing procedures each semiconductor device undergoes in accordance with the accessed data.

42. The process of claim 40, wherein the step of storing data comprises storing data that identifies repairs performed semiconductor device.

43. The process of claim 42, wherein the semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein storing data

comprises storing data that identifies spare rows and columns used in repairing the DRAM semiconductor device.

44. The process of claim 42, wherein the semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein storing data comprises storing data that identifies spare rows and columns available to effect repairs in the DRAM semiconductor device.

45. The process of claim 40, wherein the step of storing data comprises storing data at probe.

46. The process of claim 40, wherein the step of automatically reading the identification code of each semiconductor device comprises electrically retrieving a unique fuse ID programmed into each semiconductor device.

47. The process of claim 40, wherein the step of automatically reading the identification code of each semiconductor device comprises an identification code including one of fuse ID, dot code, and bar code.

48. The process of claim 40, wherein the step of automatically reading the identification code of each semiconductor device comprises a dot code.

49. The process of claim 40, wherein the step of automatically reading the identification code of each semiconductor device comprises an identification code including a bar code.

50. The process of claim 40, wherein the step of automatically reading the identification code of each semiconductor device comprises optically reading a unique ID code provided on each semiconductor device.

51. The process of claim 50, wherein the step of optically reading a unique identification code provided on each semiconductor device comprises optically reading a unique laser fuse ID programmed into each semiconductor device.

52. The process of claim 40, wherein the step of automatically reading the identification code of each semiconductor device comprises automatically reading the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the semiconductor device manufacturing process.

53. The process of claim 40, wherein the step of accessing the data stored in association with the identification code of each semiconductor device comprises accessing the data stored in association with the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the semiconductor device manufacturing process.

54. The process of claim 41, wherein selecting manufacturing procedures the semiconductor device undergoes in accordance with the accessed data comprises selecting repairs the semiconductor device undergoes in accordance with the accessed data.

55. The process of claim 54, wherein the semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein selecting repairs the semiconductor device undergoes comprises selecting spare rows and columns used to repair the DRAM semiconductor device.

56. The process of claim 41, wherein the step of selecting manufacturing procedures the semiconductor device undergoes in accordance with the accessed data comprises selecting whether the semiconductor device undergoes repair procedures.

57. The process of claim 56, wherein the semiconductor device comprise Dynamic Random Access Memory (DRAM) semiconductor device, wherein selecting whether the semiconductor device undergoes repair procedures comprises selecting whether the DRAM semiconductor device will be repaired in accordance with whether the accessed data indicates enough spare rows and columns are available in the semiconductor device to effect repairs.

58. The process of claim 41, wherein the step of selecting manufacturing procedures the semiconductor device will undergo in accordance with the accessed data comprises determining whether the semiconductor device will be assembled into Multi-Chip Modules (MCM's) in accordance with whether the accessed data indicates the semiconductor device is repairable.

59. The process of claim 40, further comprising assembling the semiconductor device into a packaged semiconductor device after the step of storing data and before the step of automatically reading the identification code of each semiconductor device.

60. A method of manufacturing semiconductor devices from wafers, the method comprising:

providing a plurality of wafers;

fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers;

causing each semiconductor device on the at least one wafer to store a substantially unique identification code;

storing data in association with the identification code of each semiconductor device that identifies manufacturing procedures the semiconductor device has undergone;

separating each semiconductor device on the at least one wafer from its wafer to form at least one semiconductor device;

assembling the at least one semiconductor device into a semiconductor device assembly;

automatically reading the identification code associated with the at least one semiconductor device; and

accessing the data stored in association with the identification code associated with the at least one semiconductor device.

61. The method of claim 60, further comprising:

selecting manufacturing procedures the at least one semiconductor device undergoes in accordance with the accessed data.

62. The method of claim 60, wherein the step of fabricating a plurality of semiconductor devices on at least one wafer comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor device, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, and processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices .

63. The method of claim 60, wherein the step of causing the semiconductor devices to store a substantially unique identification code comprises programming each semiconductor device on each of the wafers to permanently store a unique fuse ID.

64. The method of claim 60, wherein the step of causing the semiconductor devices to store a substantially unique identification code comprises applying a dot code to the semiconductor devices.

65. The method of claim 60, wherein the step of causing the semiconductor devices to store a substantially unique identification code comprises applying a bar code to the semiconductor devices.

66. The method of claim 60, wherein the step of programming each semiconductor device on each of the wafers to permanently store a unique fuse identification code comprises programming at least one of fuses and anti-fuses in each semiconductor device on each of the wafers to permanently store a unique fuse identification.

67. The method of claim 60, wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

picking each semiconductor device from its wafer;

placing each semiconductor device onto an epoxy coated bonding site of one lead frame of a plurality of lead frames;

curing the epoxy on the bonding site of each lead frame of the lead frames;

wire bonding each semiconductor device to its associated lead frame;

encapsulating each semiconductor device and its associated lead frame to form one of a plurality of semiconductor device assembly packages, each package having projecting leads;

curing each of the semiconductor device assembly packages;

de-flashing the projecting leads of each semiconductor device assembly package;

electroplating the projecting leads of each semiconductor device assembly package; and

singulating each semiconductor device assembly package into one semiconductor device assembly package of a plurality of discrete semiconductor device assembly packages.

68. The method of claim 60, wherein separating each semiconductor device on the at least one wafer from its wafer to form at least one semiconductor device wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

singulating at least one semiconductor device from the at least one wafer using a saw.

69. The method of claim 60, wherein separating each semiconductor device on the at least one wafer from its wafer to form at least one semiconductor device wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

singulating at least one semiconductor device from the at least one wafer using a laser.

70. The method of claim 60, wherein separating each semiconductor device on the at least one wafer from its wafer to form at least one semiconductor device wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

singulating at least one semiconductor device from the at least one wafer using a laser/water apparatus.

71. The method of claim 60, wherein separating each semiconductor device on the at least one wafer from its wafer to form at least one semiconductor device wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

singulating at least one semiconductor device from the at least one wafer using a cool laser apparatus.

72. The method of claim 60, wherein separating each semiconductor device on the at least one wafer from its wafer to form at least one semiconductor device wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

singulating at least one semiconductor device from the at least one wafer using a water jet apparatus.

73. The method of claim 60, wherein the step of assembling each semiconductor device into a semiconductor device assembly comprises assembling each semiconductor device into a semiconductor device assembly selected from a group comprising a wire bond/lead frame semiconductor device, a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

74. The method of claim 60, wherein the step of assembling each semiconductor device of the semiconductor dice into a semiconductor device assembly comprises:

mounting the at least one semiconductor device on one of a lead frame of a plurality of lead frames and a substrate;

encapsulating each semiconductor device and a portion of one of a lead frame and a substrate forming a semiconductor device assembly package; and

singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package.

75. The method of claim 74, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a saw.

76. The method of claim 74, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a laser.

77. The method of claim 74, wherein the step of singulating the semiconductor

device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a laser/water apparatus.

78. The method of claim 74, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a cool laser.

79. The method of claim 74, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a water jet.

80. A method of manufacturing semiconductor devices from a plurality of wafers, the method comprising:

providing a plurality of wafers;

fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers;

causing at least one semiconductor device on the at least one wafer to store a substantially unique identification code;

storing data in association with the identification code of the at least one semiconductor device identifying manufacturing procedures the at least one semiconductor device has undergone;

separating the at least one semiconductor device and at least one other semiconductor device on the at least one wafer from its wafer to form at least two semiconductor devices on a portion of the at least one wafer;

assembling the at least two semiconductor devices into a semiconductor device assembly;

automatically reading the identification code associated with the at least two semiconductor devices; and

accessing the data stored in association with the identification code associated with the at least two semiconductor devices.

81. The method of claim 80, further comprising:

selecting manufacturing procedures the at least one semiconductor device undergoes in accordance with the accessed data.

82. The method of claim 80, wherein the step of fabricating a plurality of semiconductor devices on at least one wafer comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor device, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, and processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices .

83. The method of claim 80, wherein the step of causing the at least one semiconductor device to store a substantially unique identification code comprises programming each semiconductor device on each of the wafers to permanently store a unique fuse ID.

84. The method of claim 80, wherein the step of causing the at least one semiconductor device to store a substantially unique identification code comprises applying a dot code to the semiconductor devices.

85. The method of claim 80, wherein the step of causing the at least one semiconductor device to store a substantially unique identification code comprises applying a bar code to the semiconductor devices.

86. The method of claim 83, wherein the step of programming each semiconductor device on each of the wafers to permanently store a unique fuse identification code comprises programming at least one of fuses and anti-fuses in each semiconductor device on each of the wafers to permanently store a unique fuse identification.

87. The method of claim 80, wherein the step of assembling the at least two semiconductor devices into a semiconductor device assembly comprises:
picking the at least two semiconductor devices from the wafer;
placing the at least two semiconductor devices onto a bonding site of a substrate;
encapsulating at least one semiconductor device of the at least two semiconductor devices to form one of at least one semiconductor device assembly package; and
singulating the at least one semiconductor device assembly package.

88. The method of claim 80, wherein separating the at least one semiconductor device and at least one other semiconductor device on the at least one wafer from its wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:
singulating the at least two semiconductor devices from the at least one wafer using a saw.

89. The method of claim 80, wherein separating the at least one semiconductor device and at least one other semiconductor device on the at least one wafer from its wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:
singulating the at least two semiconductor devices from the at least one wafer using a laser.

90. The method of claim 80, wherein separating the at least one semiconductor device and at least one other semiconductor device on the at least one wafer from its wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:

singulating the at least two semiconductor devices from the at least one wafer using a laser/water apparatus.

91. The method of claim 80, wherein separating the at least one semiconductor device and at least one other semiconductor device on the at least one wafer from its wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:

singulating the at least two semiconductor devices from the at least one wafer using a cool laser apparatus.

92. The method of claim 80, wherein separating the at least one semiconductor device and at least one other semiconductor device on the at least one wafer from its wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:

singulating the at least two semiconductor devices from the at least one wafer using a water jet apparatus.

93. The method of claim 80, wherein the step of assembling each semiconductor device into a semiconductor device assembly comprises assembling each semiconductor device into a semiconductor device assembly selected from a group comprising a wire bond/lead frame semiconductor device, a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

94. The method of claim 80, wherein the step of assembling the at least two semiconductor devices into a semiconductor device assembly comprises:

mounting the at least two semiconductor devices on a substrate;

encapsulating each semiconductor device and a portion of the substrate forming semiconductor device assembly packages; and

singulating the semiconductor device assembly packages.

95. The method of claim 94, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a saw.

96. The method of claim 94, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a laser.

97. The method of claim 94, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a laser/water apparatus.

98. The method of claim 94, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a cool laser.

99. The method of claim 94, wherein the step of singulating the semiconductor device assembly package from one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a water jet.

100. A method of manufacturing semiconductor devices from a plurality of wafers, the method comprising:

providing a plurality of wafers;

fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers;

causing at least one semiconductor device on the at least one wafer to store a substantially unique identification code;

storing data in association with the identification code of the at least one semiconductor device identifying manufacturing procedures the at least one semiconductor device has undergone;

assembling the at least one wafer into a semiconductor device assembly;

automatically reading the identification code associated with the at least one semiconductor device; and

accessing the data stored in association with the identification code associated with the at least one semiconductor device.

101. The method of claim 100, further comprising:

selecting manufacturing procedures the at least one semiconductor device undergoes in accordance with the accessed data.

102. The method of claim 100, wherein the step of fabricating a plurality of semiconductor devices on at least one wafer comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor device, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, and processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices.

103. The method of claim 100, wherein the step of causing the at least one semiconductor device to store a substantially unique identification code comprises programming each semiconductor device on each of the wafers to permanently store a unique fuse ID.

104. The method of claim 100, wherein the step of causing the at least one semiconductor device to store a substantially unique identification code comprises applying a dot code to the semiconductor devices.

105. The method of claim 100, wherein the step of causing the at least one semiconductor device to store a substantially unique identification code comprises applying a bar code to the semiconductor devices.

106. The method of claim 103, wherein the step of programming at least one semiconductor device on the wafer to permanently store a unique fuse identification code comprises programming at least one of fuses and anti-fuses in the at least one semiconductor device on the wafer to permanently store a unique fuse identification.

107. The method of claim 100, wherein the step of assembling the at least one wafer into a semiconductor device assembly comprises assembling the wafer into a semiconductor device assembly selected from a group comprising a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

108. The method of claim 100, wherein the step of assembling the at least one wafer into a semiconductor device assembly comprises:

mounting the wafer on a substrate; and

encapsulating the wafer and a portion of the substrate forming a wafer scale semiconductor device assembly package.